



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

09/471,877

12/23/1999

ADRIAN SFARTI

0100.9910145

8063

29153 7590 12/31/2008
ADVANCED MICRO DEVICES, INC.
C/O VEDDER PRICE P.C.
222 N.LASALLE STREET
CHICAGO, IL 60601

EXAMINER

JOHNSON, BRIAN P

ART UNIT

PAPER NUMBER

2183

MAIL DATE

DELIVERY MODE

12/31/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 09/471,877	Applicant(s) SFARTI ET AL.	
	Examiner BRIAN P. JOHNSON	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 October 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 7-14, 16, 17 and 20-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 20-27 is/are allowed.
- 6) ☒ Claim(s) 7, 10, 11, 14 and 17 is/are rejected.
- 7) ☒ Claim(s) 8, 9, 12, 13, and 16 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claims 7-14,16,17,20-27 are presented for examination. Claim 1-6,15,18,19,28-33 have been canceled.

Applicant's remarks from 16 October 2008 have been received and placed on record.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 7, 10, 11, 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over So (U.S. Patent No. 5,909,559) in view of Watts (6,023,587) in further view of Assouad (U.S. Patent No. 5,826,093).

3. So taught a system including at least : a central processing unit (CPU106 Fig.I) operable to execute operational instructions, wherein the central processing unit includes an arithmetic logic unit (CPU MMX) interoperably coupled with a data module, an instruction module, wherein the central processing unit issues a memory access request when information relating to executing one of the operational instructions is not stored within the data module or the instruction module (see the IO request and data buffer in col.39, lines 13-60, see also DRAM controller and the arbiter in col.3, lines 11-

Art Unit: 2183

30, see PCI request from CPU in co1.19, lines 9-30), and wherein the central processing unit is contained on a substrate; north bridge [North bridge 108] operably coupled to interface with memory (cache or Main memory) at a memory rate, wherein the north bridge includes a memory access request buffer interoperably coupled with a memory controller (see the RAM and the PCI bus master in col.37, lines 39-67, col.38, lines 1-50), wherein the memory access request buffer receives the memory access request from the central processing unit at the operating rate of the central processing unit, wherein the memory controller retrieves the memory access request from the memory access request buffer (see the IO request and data buffer in col.39, lines 13-60, see also DRAM controller and the arbiter in col.3, lines 11-30, see PCI request from CPU in co1.19, lines 9-30) at the memory rate (memory rate not explicitly shown, but must be memory rate otherwise would not be operative), wherein the memory controller processes the memory access request to produce a memory response that includes information stored in memory (see request queue and PCI transactions in col.37, lines 39-67, col.38, lines 1-8), and, a bus operably coupled to the central processing unit [CPU 106] and the north bridge (see connection between CPU 106 and north bridge 108 in fig.I), wherein the bus provides a transport medium for memory access requests and corresponding memory responses between the central processing unit and the north bridge at the operating rate of the central processing unit (not explicitly shown, but see CPU MMX operating rate as known in the art), and wherein the bus is contained on the substrate.

Art Unit: 2183

4. So did not specifically show the programmable phase locked loop that provides an operating rate for the central processing unit. However, Watts Jr (6,023,587) taught programmable phase locked loop that provides an operating rate for the central processing unit [CPU] (see the clock rate of phase locked loop to CPU in col 1.14, lines 43-47). It would have been obvious to one of ordinary skill in the art to use Watts in So for including the programmable phase locked loop that provides an operating rate for the central processing unit as claimed because the use of Watts could provide So the ability to control the clock intervals at a predefined set of system requirement, and one of ordinary skill in the art should be able to recognize the advantage of using the programmable phase locked loop as adjustable CPU internal clock. As to claims 10,17, So did not specifically show the physical address as claimed. However, since no specific format of physical address has been reflected in the claim, examiner holds that generation of physical address in general had been known in the art.

5. So/Watts fails to disclose that the Northbridge is integrated into the substrate.

Assouad discloses a memory controller within the integrate circuit (col 2 lines 43-49).

So/Watts would have been motivated to allow an integrated memory controller for performance and efficiency advantages.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of So/Watts and incorporate the Northbridge on an integrated circuit, as in Assouad.

6. As to claim 11, So also included a memory bus coupled to north bridge (see bus connected to the north bridge and the memory in fig. 1).

Allowable Subject Matter

7. Claims 8, 9, 12, 13, and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claims 20-27 are allowed.

Response to Arguments

9. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

10. Applicant further argues:

In addition, the claim requires, among other things, that the memory access request from the central processing unit is done at an operating rate of the processing unit wherein the memory controller receives memory access request from the memory access request buffer. The office action cites column 39, lines 13-60 as allegedly teaching this subject matter, however no such teaching can be found. The teaching actually refers to a DSP, not a CPU and a PCI bus. A PCI bus as known in the art does not operate at an operating rate of a central processing unit. Other differences will be recognized by those of ordinary skill in the art."

The claimed "operating rate" is quite vague and, thus, interpreted quite broadly. Without improperly reading limitations from the specification into the claims, it is impossible to determine from the language what patentable weight to give the term

Art Unit: 2183

“operating rate.” Indeed, absent this clarification, the operating rate is interpreted to be the same if these elements can communicate in sync.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BRIAN P. JOHNSON whose telephone number is (571)272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2183

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Brian Johnson/ Patent Examiner, Art Unit 2183

/Eric Coleman/
Primary Examiner, Art Unit 2183